DALLAS
SEMICONDUCTOR

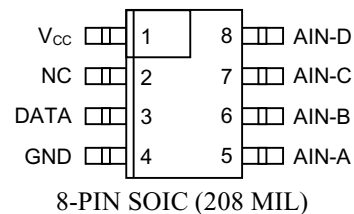# DS2450
1-Wire™ Quad A/D Converter

FEATURES

- Four high-impedance inputs to measure analog voltages over the 1-Wire bus
- User programmable input range (2.56V, 5.12V), resolution (1 to 16 bits) and alarm thresholds
- 5V, single supply operation
- Very low power: 2.5 mW active, 25 µW idle
- Built-in multidrop controller allows multiple DS2450's to be identified and operated on a common 1-Wire bus
- Responds to Conditional Search if the analog voltage crosses the alarm thresholds
- Channels not used as analog input can serve as open drain digital outputs for closed-loop control
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- Overdrive mode boosts communication speed to 142k bits per second
- On-chip 16-bit CRC-generator for safeguarding data transfers
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number 8-bit CRC tester) assures absolute traceability because no two parts are alike
- 8-bit family code specifies device communication requirements to bus master
- Operating temperature range from -40°C to +85°C
- Compact, low cost 8-pin SOIC surface mount package

PIN ASSIGNMENT

V_{CC}	1	8	AIN-D
NC	2	7	AIN-C
DATA	3	6	AIN-B
GND	4	5	AIN-A

8-PIN SOIC (208 MIL)

PIN DESCRIPTION

V_{CC}	4.5 to 5.5V
NC	Do Not Connect
DATA	1-Wire Bus
GND	Ground
AIN-A	Analog Input A
AIN-B	Analog Input B
AIN-C	Analog Input C
AIN-D	Analog Input D

ORDERING INFORMATION

DS2450S   8-pin SOIC

DESCRIPTION

The DS2450 1-Wire Quad A/D Converter is based on a successive-approximation analog to digital converter with a four to one analog multiplexer. Each input channel has its own register set to store the input voltage range, resolution, and alarm threshold values as well as flags to enable participation of the device in the conditional search if the input voltage leaves the specified range. Two alarm flags for each channel indicate if the voltage measured was too high or too low without requiring the bus master to do

the comparison. Each A/D conversion is initiated by the bus master. A channel not used as analog input can serve as a digital open-drain output. After disabling the input the bus master can directly switch on or off the open-drain transistor at the selected channel. All device settings are stored in SRAM and kept non-volatile while the device gets power either through the 1-Wire bus or through its V_{CC} pin. After powering up a power-on reset flag signals the bus master the need to restore the device settings before the regular operation can resume. All device registers and conversion read-out registers are organized as three 8-byte memory pages similar to the Status Memory of a DS2505/6 device. An on-chip CRC16 generator protects the communication against transmission errors when reading through the end of a memory page as well as when writing individual bytes.

OVERVIEW

The block diagram in Figure 1 shows the major function blocks of the device. The DS2450 contains a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit family code (20H). The 64-bit ROM portion of the DS2450 not only creates an absolutely unique electronic identification for the device itself but also is a means to locate and address the device in order to exercise its control functions.

The device gets its power either from the 1-Wire bus or through its V_{CC} pin. Without a V_{CC} supply the device stores energy on an internal capacitor during periods where the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1-Wire line until it returns to high to replenish the parasite (capacitor) supply. This, however, provides sufficient energy only for communication. To perform an A/D conversion a strong pullup of the 1-Wire bus to 5V or a V_{CC} supply is required.

DS2450 BLOCK DIAGRAM Figure 1
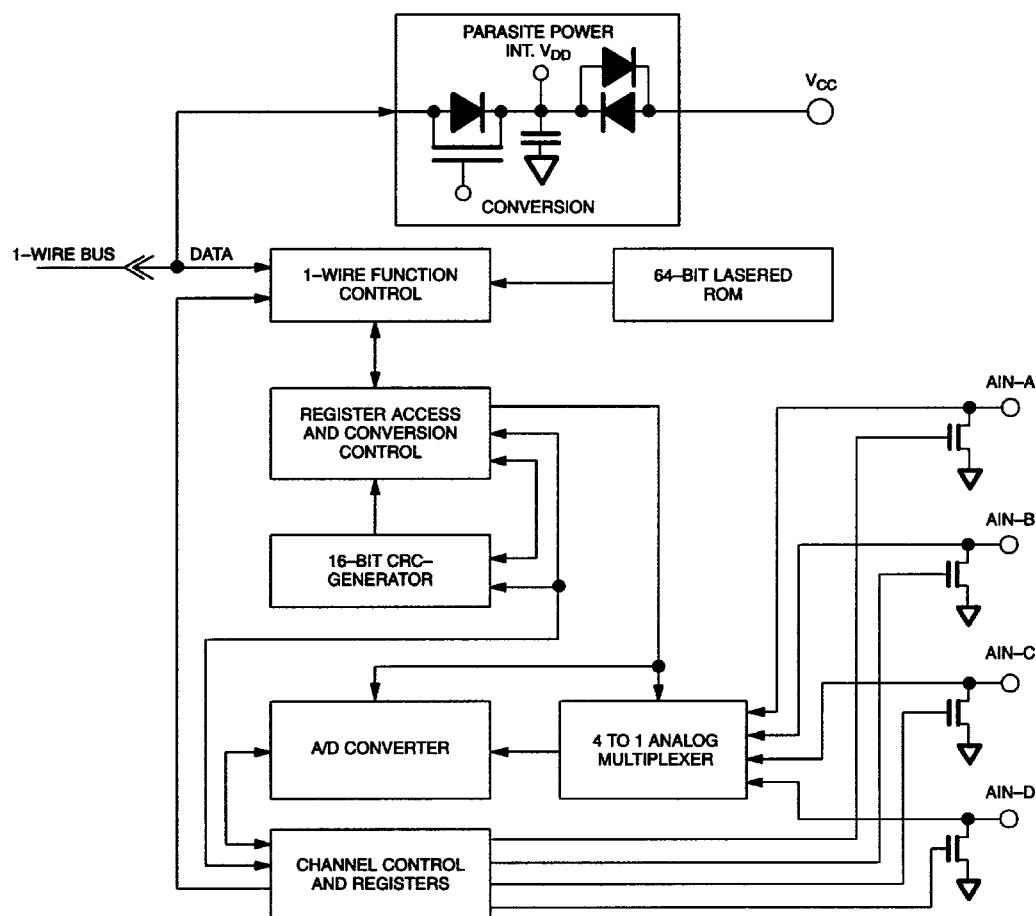
## HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2
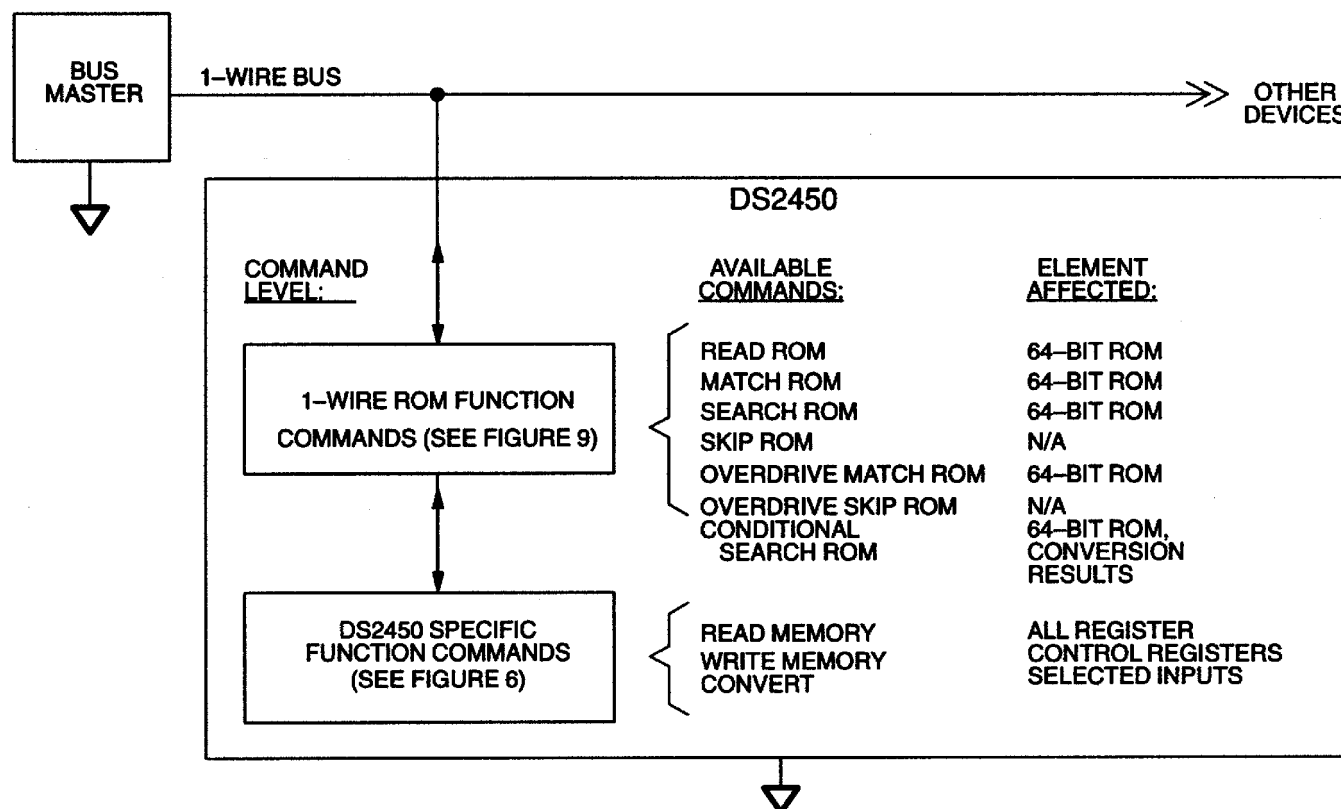
The DS2450 uses the standard Dallas Semiconductor 1-Wire protocol for data transfers. Communication to and from the DS2450 requires a single bi-directional line that is typically a port pin of a microcontroller. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The 1-Wire bus master must first provide one of the seven ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM or 7) Overdrive-Match ROM. Upon completion of an overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory and control functions become accessible and the master may provide any one of the available commands. The protocol for these commands is described in Figure 6. All data is read and written least significant bit first.
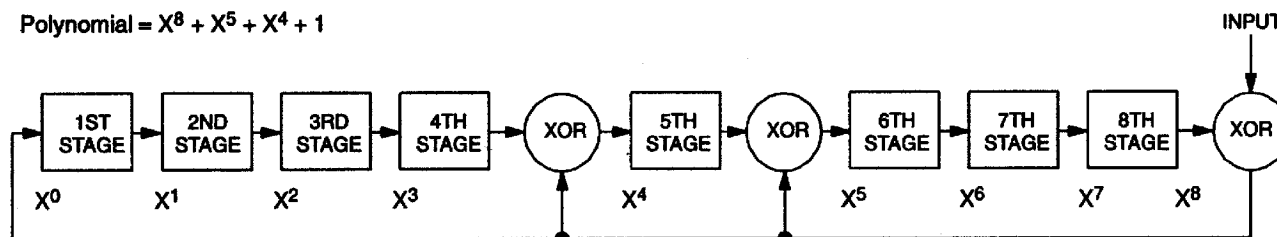
64-BIT LASERED ROM

Each DS2450 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton™ Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

64-BIT LASERED ROM Figure 3

MSB   LSB

| 8–BIT CRC CODE | 48–BIT SERIAL NUMBER | 8–BIT FAMILY CODE (20H) |

MSB   LSB   MSB   LSB   MSB   LSB
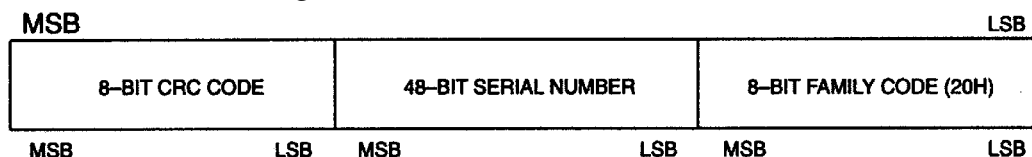
1-WIRE CRC-GENERATOR Figure 4

Polynomial = $X^8 + X^5 + X^4 + 1$ INPUT

DEVICE REGISTERS

All registers of the DS2450 are mapped into a linear memory range of 24 adjacent bytes organized as three 8-byte pages. The first page, called conversion read-out, contains the memory area where the chip-internal logic places the results of a conversion for the bus master to read. Starting with channel A at the lowest address, each channel has an area of 16 bits assigned for the conversion result, as shown in Figure 5a. The power-on default for the conversion read-out registers is all zeros. Regardless of the resolution requested, the most significant bit of the conversion is always at the same bit position. If less than 16-bit resolution is requested, the least significant bits of the conversion result will be filled with zeros in order to always generate a 16-bit result. For applications that require less than four analog inputs, one should start using input D for the first channel, input C for the second one, etc. The advantage is that when reading the conversion results one reaches the end of the page and with it the CRC16 sooner and minimizes the traffic on the 1-Wire bus. For more details on reading please refer to the Read Memory command description.

MEMORY MAP PAGE 0, CONVERSION READ-OUT Figure 5a

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	A	A	A	A	A	A	A	LSBIT A
01	MSBIT A	A	A	A	A	A	A	A
02	B	B	B	B	B	B	B	LSBIT B
03	MSBIT B	B	B	B	B	B	B	B
04	C	C	C	C	C	C	C	LSBIT C
05	MSBIT C	C	C	C	C	C	C	C
06	D	D	D	D	D	D	D	LSBIT D
07	MSBIT D	D	D	D	D	D	D	D

The control and status information for all channels is located in memory page 1 (Figure 5b). As for the conversion read-out, each channel has assigned 16 bits. The four least significant bits, called RC3 to RC0, are an unsigned binary number that represents the number of bits to be converted. A code of 1111 (15 decimal) will generate a 15-bit result. For a full 16-bit conversion the code number needs to be 0000. The next two bits beyond RC3 will always read 0. They have no function and cannot be changed to 1s.

The next bits, OC (output control) and OE (enable output) control the alternate use of a channel as output. For normal operation as analog input the OE bit of a channel needs to be 0, rendering the OC bit to a don't care. With OE set to 1, a 0 for OC will make the channel's output transistor conducting, a 1 for OC will switch the transistor off. With a pullup resistor to a positive voltage, for example, the OC bit will directly translate into the voltage equivalent of its logic state. Enabling the output does not disable the analog input. Conversions remain possible, but will result in values close to 0 if the transistor is conducting.

The IR bit in the second byte of a channel's control and status memory selects the input voltage range. With IR set to 0, the highest possible conversion result is reached at 2.55V. Setting IR to 1 requires an input voltage of 5.10V for the same result. The next bit beyond IR has no function. It will always read 0 and cannot be changed to 1.

The next two bits, AEL alarm enable low and AEH alarm enable high, control whether the device will respond to the Conditional Search command (see ROM Functions) if a conversion results in a value higher (AEH) than or lower (AEL) than the channel's alarm threshold voltage as specified in the alarm settings. The alarm flags AFL (low) and AFH (high) tell the bus master whether the channel's input voltage was beyond the low or high threshold at the latest conversion. These flags are cleared automatically if a new conversion reveals a non-alarming value. They can alternatively be written to 0 by the bus master without a conversion.

The next bit of a channel's control and status memory always reads 0 and cannot be changed to 1. The POR bit (power on reset) is automatically set to 1 as the device performs a power-on reset cycle. As long as this bit is set the device will always respond to the Conditional Search command in order to notify the bus master that the control and threshold data is no longer valid. After powering-up the POR bit needs to be written to 0 by the bus master. This may be done together with restoring the control and threshold data. It is possible for the bus master to write the POR bit to a 1. This will make the device participate in the conditional search but will **not** generate a reset cycle. Since the POR bit is related to the device and not channel-specific the value written with the most recent setting of an input range or alarm enable applies. The power-on default setting for the control/status data is 08h for the first and 8Ch for the second byte of each channel.

MEMORY MAP PAGE 1, CONTROL/STATUS DATA Figure 5b

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	OE-A	OC-A	0	0	RC3-A	RC2-A	RC1-A	RC0-A
09	POR	0	AFH-A	AFL-A	AEH-A	AEL-A	0	IR-A
0A	OE-B	OC-B	0	0	RC3-B	RC2-B	RC1-B	RC0-B
0B	POR	0	AFH-B	AFL-B	AEH-B	AEL-B	0	IR-B
0C	OE-C	OC-C	0	0	RC3-C	RC2-C	RC1-C	RC0-C
0D	POR	0	AFH-C	AFL-C	AEH-C	AEL-C	0	IR-C
0E	OE-D	OC-D	0	0	RC3-D	RC2-D	RC1-D	RC0-D
0F	POR	0	AFH-D	AFL-D	AEH-D	AEL-D	0	IR-D

MEMORY MAP PAGE 2, ALARM SETTINGS Figure 5c

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	MSBL-A	A	A	A	A	A	A	LSBL-A
11	MSBH-A	A	A	A	A	A	A	LSBH-A
12	MSBL-B	B	B	B	B	B	B	LSBL-B
13	MSBH-B	B	B	B	B	B	B	LSBH-B
14	MSBL-C	C	C	C	C	C	C	LSBL-C
15	MSBH-C	C	C	C	C	C	C	LSBH-C
16	MSBL-D	D	D	D	D	D	D	LSBL-D
17	MSBH-D	D	D	D	D	D	D	LSBH-D

The registers for the alarm threshold voltages of each channel are located in memory page 2 with the low threshold being at the lower address (Figure 5c). The power-on default thresholds are 00h for low alarm and FFh for high alarm. The alarm settings are always eight bits. For a resolution higher or equal to eight bits the alarm flag will be set if the eight most significant bits of the conversion result yield a number higher than stored in the high alarm register (AFH) or lower than stored in the low alarm register (AFL). For a resolution lower than eight bits the least significant bits of the alarm registers are ignored.

There is a fourth memory page in the address range of 18 to 1F used during calibration at the factory. This memory page is accessible to the user through the Read Memory and Write Memory commands. Changing the data of this page arbitrarily will de-calibrate the A/D converter or make the device nonfunctional until it undergoes a power-on reset. **If the device is VCC powered the analog circuitry must be kept permanently active** by writing a value of 40 hex to memory address 1C after power-up. This also eliminates the offset time otherwise needed with each CONVERT command. See the description of the CONVERT command for details.

FUNCTION COMMANDS
The Function Command Flow Chart (Figure 6) describes the protocols necessary for accessing the device registers. Since the memory map of the DS2450 is small compared to the 16-bit addressing capabilities the 11 most significant bits of the address will be forced to 0 before they enter the CRC-generator. The communication between master and DS2450 takes place either at regular speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into Overdrive mode the device assumes regular speed.

READ MEMORY [AAH]
The Read Memory command is used to read conversion results, control/status data and alarm settings. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the memory map. With every subsequent read data time slot the bus master receives data from the DS2450 starting at the supplied address and continuing until the end of an eight-byte page is reached. At that point the bus master will receive a 16-bit CRC of the command byte, address bytes and data bytes. This CRC is computed by the DS2450 and read back by the bus master to check if the command word, starting address and data were received correctly. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated.

Note that the initial pass through the Read Memory flow chart will generate a 16-bit CRC value that is the result of clearing the CRC-generator and then shifting in the command byte followed by the two address bytes, and finally the data bytes beginning at the first addressed memory location and continuing through to the last byte of the addressed page. Subsequent passes through the Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC-generator and then shifting in the new data bytes starting at the first byte of the next page.
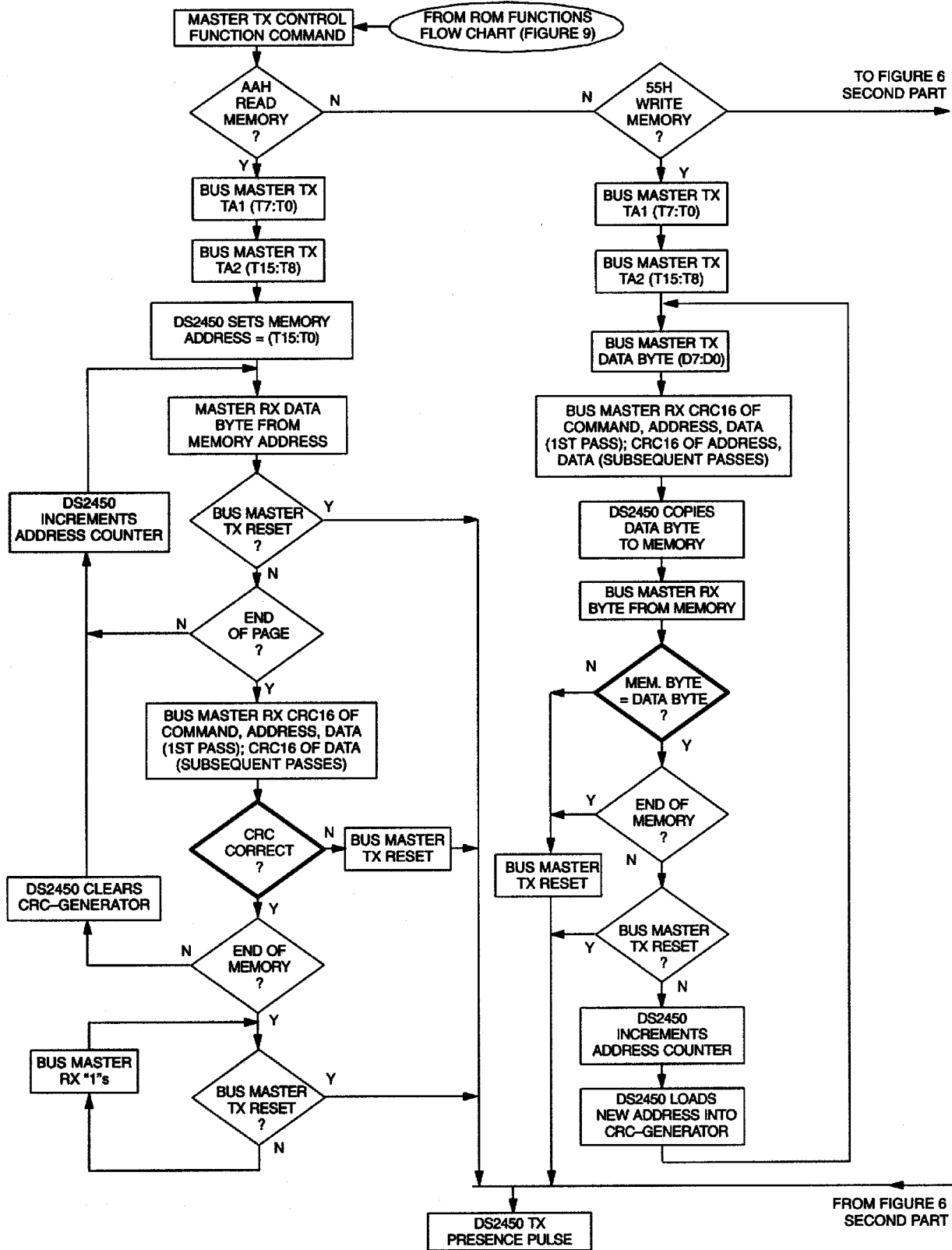
WRITE MEMORY [55H]

The Write Memory command is used to write to memory pages 1 and 2 in order to set the channel-specific control data and alarm thresholds. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a data byte of (D7:D0). A 16-bit CRC of the command byte, address bytes, and data byte is computed by the DS2450 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received. Now the DS2450 copies the data byte to the specified memory location. With the next eight time slots the bus master receives a copy of the same byte but read from memory for verification. If the verification fails, a Reset Pulse should be issued and the current byte address should be written again.

If the bus master does not issue a Reset Pulse and the end of memory was not yet reached, the DS2450 will automatically increment its address counter to address the next memory location. The new two-byte address will also be loaded into the 16-bit CRC-generator as a starting value. The bus master will send the next byte using eight write time slots. As the DS2450 receives this byte it also shifts it into the CRC-generator and the result is a 16-bit CRC of the new data byte and the new address. With the next sixteen read time slots the bus master will read this 16-bit CRC from the DS2450 to verify that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse should be issued in order to repeat the Write Memory command sequence.
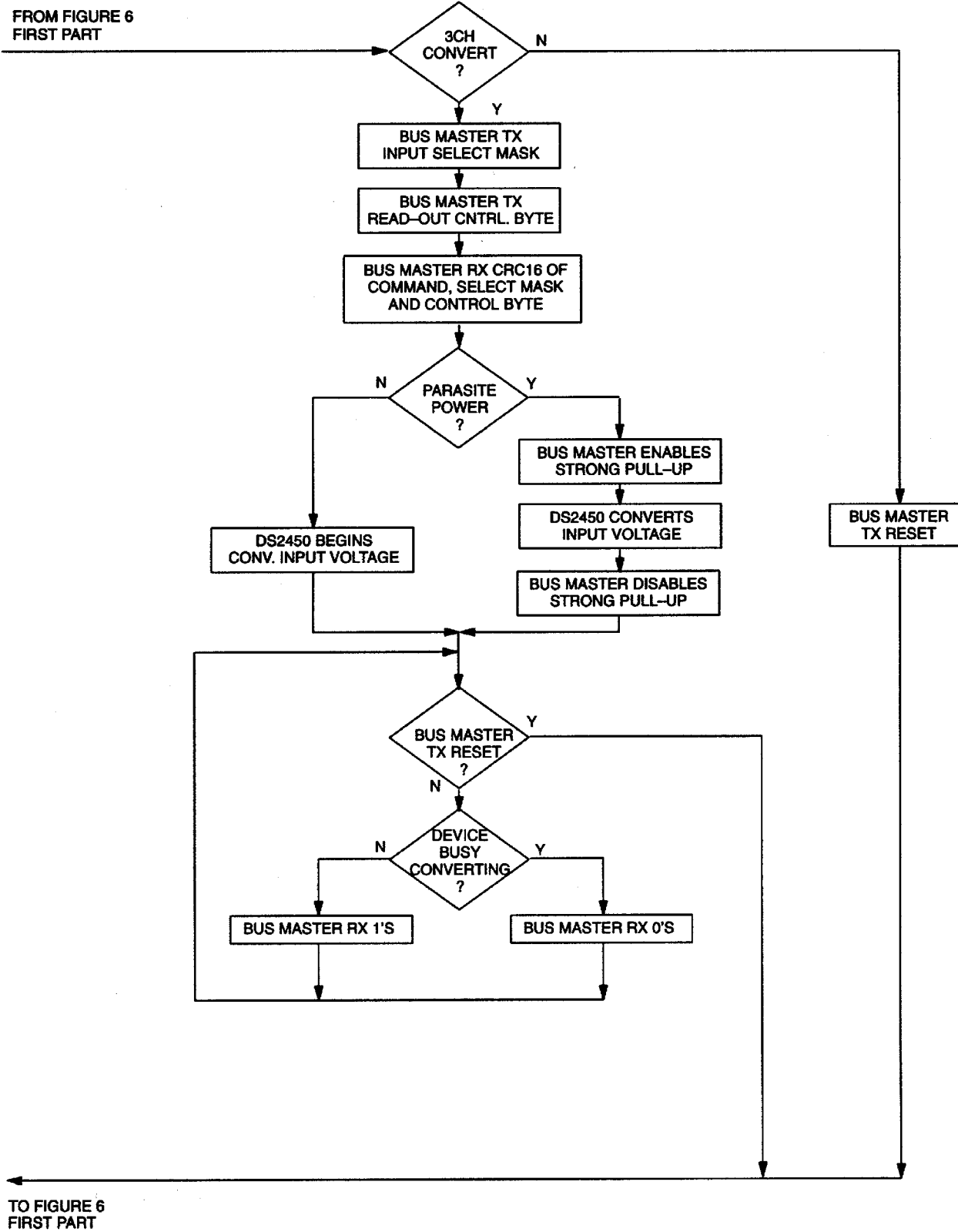
Note that the initial pass through the Write Memory flow chart will generate a 16-bit CRC value that is the result of shifting the command byte into the CRC-generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS2450 automatically incrementing its address counter will generate a 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC-generator and then shifting in the new data byte.

The decision to continue after having received a bad CRC or if the verification fails is made entirely by the bus master. Write access to the conversion read-out registers is not possible. If a write attempt is made to a page 0 address the device will follow the Write Memory flow chart correctly but the verification of the data byte read back from memory will usually fail. The Write Memory command sequence can be ended at any point by issuing a Reset Pulse.

FUNCTION COMMAND FLOW CHART Figure 6

MASTER TX CONTROL FUNCTION COMMAND

FROM ROM FUNCTIONS FLOW CHART (FIGURE 9)

AAH READ MEMORY ?

55H WRITE MEMORY ?

TO FIGURE 6 SECOND PART

BUS MASTER TX TA1 (T7:T0)

BUS MASTER TX TA2 (T15:T8)

DS2450 SETS MEMORY ADDRESS = (T15:T0)

MASTER RX DATA BYTE FROM MEMORY ADDRESS

DS2450 INCREMENTS ADDRESS COUNTER

BUS MASTER TX RESET ?

END OF PAGE ?

BUS MASTER RX CRC16 OF COMMAND, ADDRESS, DATA (1ST PASS); CRC16 OF DATA (SUBSEQUENT PASSES)

DS2450 CLEARS CRC-GENERATOR

CRC CORRECT ?

BUS MASTER TX RESET

END OF MEMORY ?

BUS MASTER RX "1"s

BUS MASTER TX RESET ?

BUS MASTER TX TA1 (T7:T0)

BUS MASTER TX TA2 (T15:T8)

BUS MASTER TX DATA BYTE (D7:D0)

BUS MASTER RX CRC16 OF COMMAND, ADDRESS, DATA (1ST PASS); CRC16 OF ADDRESS, DATA (SUBSEQUENT PASSES)

DS2450 COPIES DATA BYTE TO MEMORY

BUS MASTER RX BYTE FROM MEMORY

MEM. BYTE = DATA BYTE ?

END OF MEMORY ?

BUS MASTER TX RESET

BUS MASTER TX RESET ?

DS2450 INCREMENTS ADDRESS COUNTER

DS2450 LOADS NEW ADDRESS INTO CRC-GENERATOR

FROM FIGURE 6 SECOND PART

DS2450 TX PRESENCE PULSE

FUNCTION COMMAND FLOW CHART Figure 6 (continued)

CONVERT [3CH]

The Convert command is used to initiate the analog to digital conversion for one or more channels at the resolution specified in memory page 1, control/status data. The conversion takes between 60 and 80 μs per bit plus an offset time of maximum 160 μs every time the convert command is issued. For four channels with 12-bit resolution each, as an example, the convert command will not take more than 4x12x80 μs plus 160 μs offset, which totals 4 ms. If the DS2450 gets its power through the V_{CC} pin, the bus master may communicate with other devices on the 1-Wire bus while the DS2450 is busy with A/D conversions. If the device is powered entirely from the 1-Wire bus, the bus master must instead provide a strong pullup to 5V for the estimated duration of the conversion in order to provide sufficient energy.

The conversion is controlled by the input select mask (Figure 7a) and the read-out control byte (Figure 7b). In the input select mask the bus master specifies which channels participate in the conversion. A channel is selected if the bit associated to the channel is set to 1. If more than one channel is selected, the conversion takes place one channel after another in the sequence A, B, C, D, skipping those channels that are not selected. The bus master can read the result of a channel's conversion before the conversion of all the remaining selected channels is completed. In order to distinguish between the previous result and the new value the bus master uses the read-out control byte. This byte allows presetting the conversion read-out registers for each selected channel to all 1's or all 0's. If the expected result is close to 0 then one should preset to all 1's or to all 0's if the conversion result will likely be a high number. In applications where the bus master can wait until all selected channels are converted before reading, a preset of the read-out registers is not necessary. **Note** that for a channel not selected in the input select mask, the channel's read-out control setting has no effect. If a channel constantly yields conversion results close to 0 the channel's output transistor may be conducting. See section Device Registers for details.

INPUT SELECT MASK (CONVERSION COMMAND) Figure 7a

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
"don't care"				D	C	B	A

READ-OUT CONTROL (CONVERSION COMMAND) Figure 7b

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Set D	Clear D	Set C	Clear C	Set B	Clear B	Set A	Clear A

Set	Clear	Explanation
0	0	no preset, leave as is
0	1	preset to all 0's
1	0	preset to all 1's
1	1	(illegal code)

Following the Convert command byte the bus master transmits the input select mask and the read-out control byte. Now the bus master reads the CRC16 of the command byte, select mask and control byte. The conversion will start no earlier than 10 μs after the most significant bit of the CRC is received by the bus master.

With a parasitic power supply the bus master must activate the strong pullup within this 10 μs window for a duration that is estimated as explained above. After that, the data line returns to an idle high state and communication on the bus can resume. The bus master would normally send a reset pulse to exit the Convert command. Read data time slots generated after the strong pullup has ended but before issuing a reset pulse should result in all 1's if the conversion time was calculated correctly.

With V_{CC} power supply the bus master may either send a reset pulse to exit the Convert command or continuously generate read data time slots. As long as the DS2450 is busy with conversions the bus master will read 0's. After the conversion is completed the bus master will receive 1's instead. Since in a open-drain environment a single 0 overwrites multiple 1's the bus master can monitor multiple devices converting simultaneously and immediately knows when the last one is ready. As in the parasitically powered scenario the bus master finally has to exit the Convert command by issuing a rest pulse.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS2450 is a slave device. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2450 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3k bits per second. The speed can be boosted to 142k bits per second by activating the Overdrive Mode. The 1-Wire bus requires a pullup resistor of approximately 5kΩ at regular speed or maximum 2.2kΩ at Overdrive speed for communication. During A/D conversions the bus master must provide a strong pullup to 5V to supply sufficient energy if the DS2450 is powered entirely from the 1-Wire bus.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 μs (Overdrive Speed) or more than 120 μs (regular speed), one or more devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8
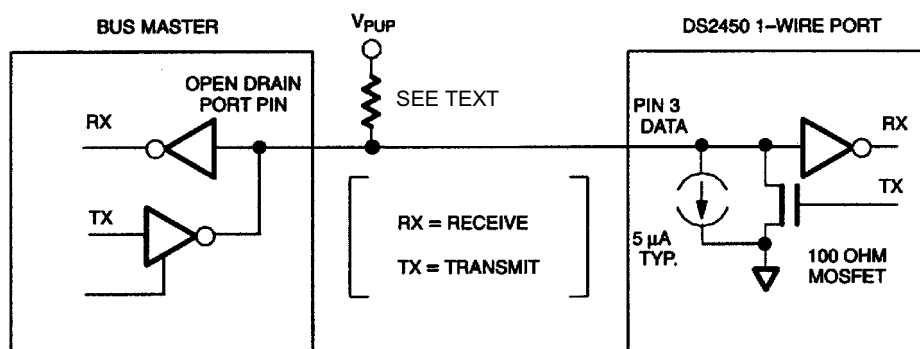
TRANSACTION SEQUENCE

The protocol for accessing the DS2450 via the 1-Wire port is as follows:
- Initialization
- ROM Function Command
- Memory/Convert Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2450 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33H]

This command allows the bus master to read the DS2450's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2450 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

MATCH ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2450 on a multidrop bus. Only the DS2450 that exactly matches the 64-bit ROM sequence will respond to the following memory/convert function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SKIP ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory/ convert functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

SEARCH ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a Search ROM, including an actual example.

CONDITIONAL SEARCH [ECH]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition will participate in the search. The DS2450 will respond to the Conditional Search command if a channel's alarm enable flags AEH and/or AEL are set and the conversion results in a value outside the range specified by the channel's alarm threshold voltages. See section Device Registers for details. The Conditional Search ROM provides an efficient means for the bus master to determine devices on a multidrop system that have to signal an important event, such as a voltage leaving the tolerance band. After each pass of the Conditional Search that successfully determined the 64-bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued since all other devices will have dropped out of the search process and are waiting for a reset pulse.

OVERDRIVE SKIP ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory/convert functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2450 in the Overdrive Mode (OD = 1). All communication following this command has to occur at Overdrive Speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD = 0).

When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Overdrive Match ROM [69H]

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS2450 on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS2450 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

ROM FUNCTIONS FLOW CHART Figure 9
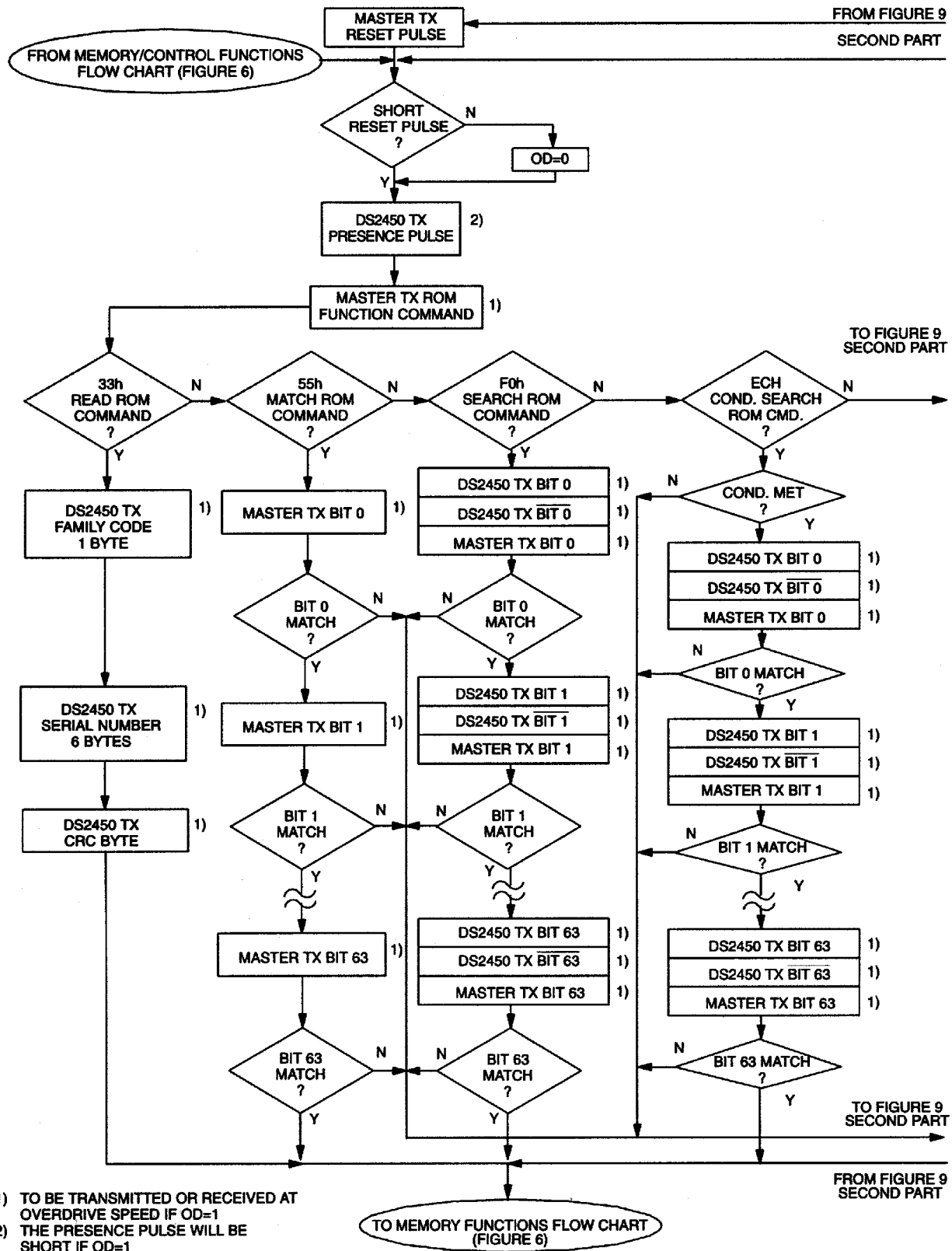
ROM FUNCTIONS FLOW CHART Figure 9 (continued)
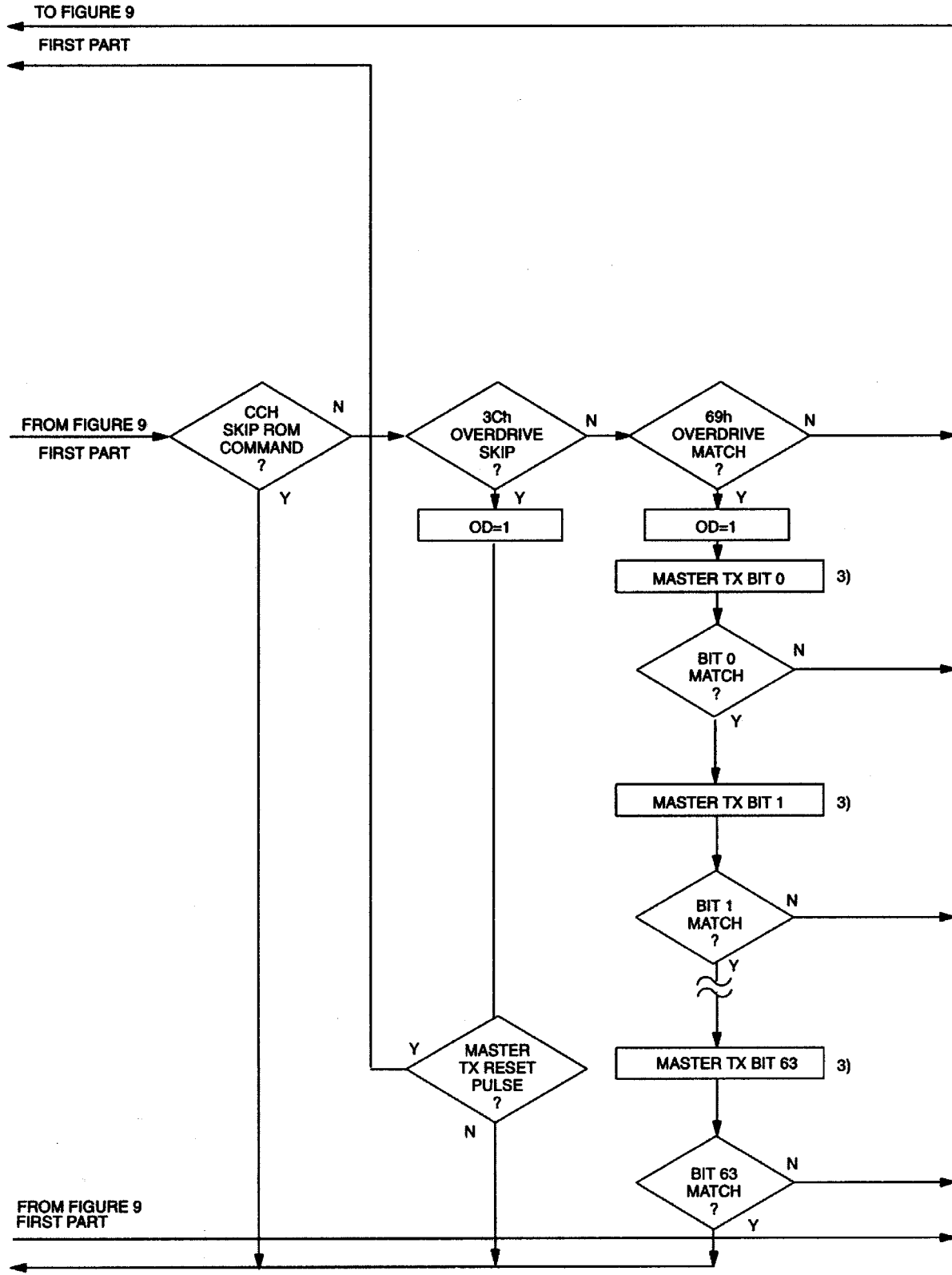
USAGE EXAMPLE (set-up section)

There is a single V_{CC} powered DS2450 on the 1-Wire bus. Set-up channel D for 12 bits, 5.12V range and alarm thresholds of 2.0V (64h) and 3.0V (96h) (increment 20 mV) and convert the input voltage; turn on the channel A output if low alarm occurs and the channel B output if high alarm occurs, respectively.

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
TX	Reset	Reset Pulse (480 - 960 μs)	
RX	Presence	Presence Pulse	
TX	CCh	Issue "Skip ROM" Command	
TX	55h	Issue "Write Memory" Command	
TX	08h	TA1, beginning address	
TX	00h	TA2, address = 0008h	
TX	C0h	data byte (address 0008)	**CH-A**
RX	<CRC16>	CRC of command, address, data byte	
RX	C0h	read-back for simple verification	
TX	00h	next data byte (address 0009h)	
RX	<CRC16>	CRC of address, data byte	
RX	00h	read-back for simple verification	
TX	C0h	data byte (address 000A)	**CH-B**
RX	<CRC16>	CRC of address, data byte	
RX	C0h	read-back for simple verification	
TX	00h	next data byte (address 000Bh)	
RX	<CRC16>	CRC of address, data byte	
RX	00h	read-back for simple verification	
TX	C0h	data byte (address 000C)	**CH-C***
RX	<CRC16>	CRC of address, data byte	
RX	C0h	read-back for simple verification	
TX	00h	next data byte (address 000Dh)	
RX	<CRC16>	CRC of address, data byte	
RX	00h	read-back for simple verification	
TX	0Ch	data byte (address 000E)	**CH-D**
RX	<CRC16>	CRC of address, data byte	
RX	0Ch	read-back for simple verification	
TX	0Dh	next data byte (address 000Fh)	
RX	<CRC16>	CRC of address, data byte	
RX	0Dh	read-back for simple verification	

Continued on the next page.

*In a multi-drop environment it takes less time to set-up an unused channel rather than skipping it.

USAGE EXAMPLE (set-up continued, conversion, read flags)

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
TX	Reset	Reset Pulse (480 - 960 µs)	
RX	Presence	Presence Pulse	
TX	CCh	Issue "Skip ROM" Command	
TX	55h	Issue "Write Memory" Command	
TX	16h	TA1, beginning address	
TX	00h	TA2, address = 0016h	
TX	64h	data byte (address 0016)	**CH-D**
RX	<CRC16>	CRC of command, address, data byte	
RX	64h	read-back for simple verification	
TX	96h	next data byte (address 0017h)	
RX	<CRC16>	CRC of address, data byte	
RX	96h	read-back for simple verification	
TX	Reset	Reset Pulse (480 - 960 µs)	
RX	Presence	Presence Pulse	
TX	CCh	Issue "Skip ROM" Command	
TX	3Ch	Issue "Convert" Command	
TX	08h	input select mask	**CH-D**
TX	40h	read-out control byte	
RX	<CRC16>	CRC of command, mask, control byte	
RX	<multiple data bytes>	continue reading until byte is FFh	
TX	Reset	Reset Pulse (480 - 960 µs)	
RX	Presence	Presence Pulse	
TX	CCh	Issue "Skip ROM" Command	
TX	Aah	Issue "Read Memory" Command	
TX	0Fh	TA1, beginning address	
TX	00h	TA2, address = 000Fh	
RX	<data byte>	status data*	**CH-D**
RX	<CRC16>	CRC of command, address, data byte	

Continued on the next page.

*The status data byte includes the channel D alarm flags AFH and AFL which are used to control the channel A and B outputs (see next page).

USAGE EXAMPLE (control channel A and channel B outputs)

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
TX	Reset	Reset Pulse (480 - 960 µs)	
RX	Presence	Presence Pulse	
TX	CCh	Issue "Skip ROM" Command	
TX	55h	Issue "Write Memory" Command	
TX	08h	TA1, beginning address	
TX	00h	TA2, address = 0008h	
TX	80h if AFL = 1 / C0h if AFL = 0	data byte (address 0008)	**CH-A**
RX	<CRC16>	CRC of command, address, data byte	
RX	<data byte>	read-back for simple verification	
TX	00h	next data byte (address 0009h)*	
RX	<CRC16>	CRC of address, data byte	
RX	00h	read-back for simple verification	
TX	80h if AFH = 1 / C0h if AFH = 0	data byte (address 000A)	**CH-B**
RX	<CRC16>	CRC of address, data byte	
RX	<data byte>	read-back for simple verification	
TX	Reset	Reset Pulse (480 - 960 µs)	
RX	Presence	Presence Pulse	

*In a multi-drop environment it takes less time to perform a non-changing write cycle rather than skipping a byte.
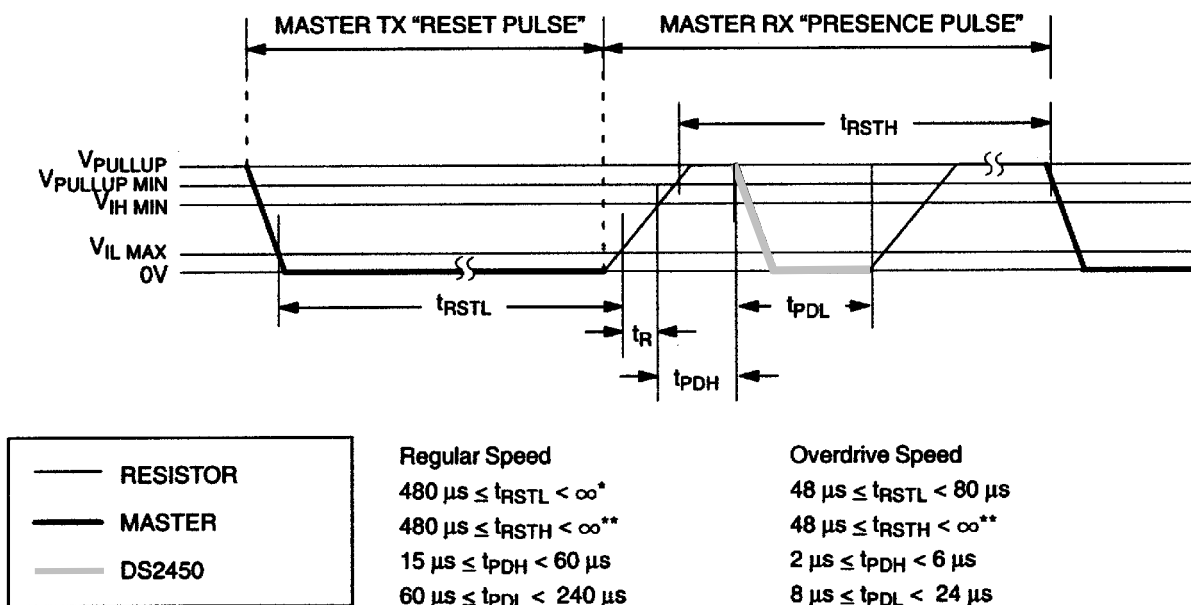
1-WIRE SIGNALING

The DS2450 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The DS2450 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS2450 will communicate at regular speed. While in Overdrive mode the fast timing applies to all wave forms.

The initialization sequence required to begin any communication with the DS2450 is shown in Figure 10. A Reset Pulse followed by a Presence Pulse indicates the DS2450 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2450 waits (t_{PDH},15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the Presence Pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive Speed).

A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2450 is in Overdrive Mode and the Reset Pulse is no longer than 80 µs the device will remain in Overdrive Mode.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PLUSES" Figure 10

	Regular Speed	Overdrive Speed
—— RESISTOR	$480\ \mu s \leq t_{RSTL} < \infty^*$	$48\ \mu s \leq t_{RSTL} < 80\ \mu s$
—— MASTER	$480\ \mu s \leq t_{RSTH} < \infty^{**}$	$48\ \mu s \leq t_{RSTH} < \infty^{**}$
—— DS2450	$15\ \mu s \leq t_{PDH} < 60\ \mu s$	$2\ \mu s \leq t_{PDH} < 6\ \mu s$
	$60\ \mu s \leq t_{PDL} < 240\ \mu s$	$8\ \mu s \leq t_{PDL} < 24\ \mu s$

*IN ORDER NOT TO MASK INTERRUPT SIGNALING BY OTHER DEVICES ON THE 1-WIRE BUS, $t_{RSTL} + t_R$ SHOULD ALWAYS BE LESS THAN 960 μs
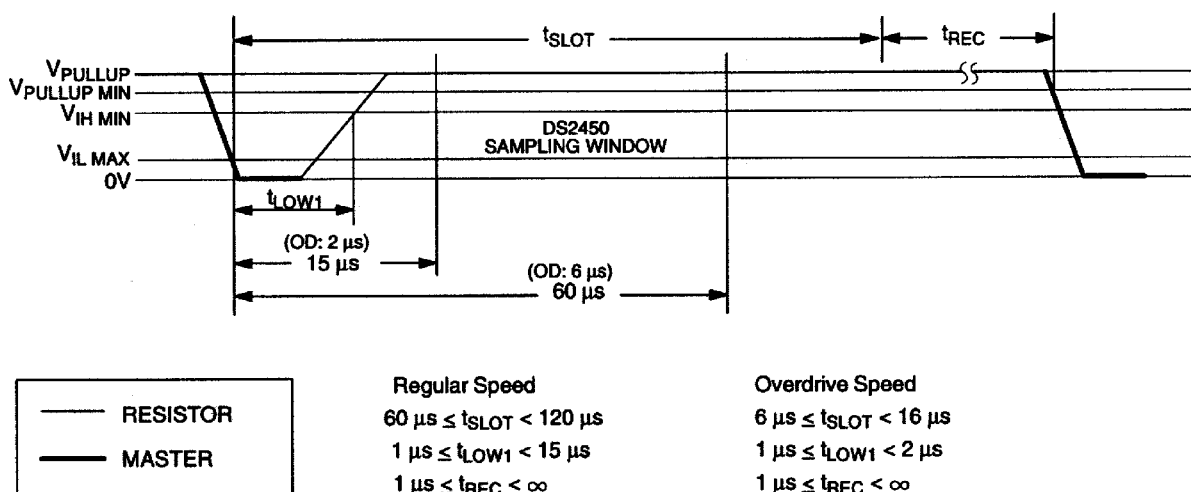**INCLUDES RECOVERY TIME

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2450 to the master by triggering a delay circuit in the DS2450. During write time slots, the delay circuit determines when the DS2450 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2450 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the device will leave the read data time slot unchanged.
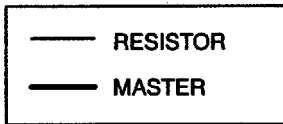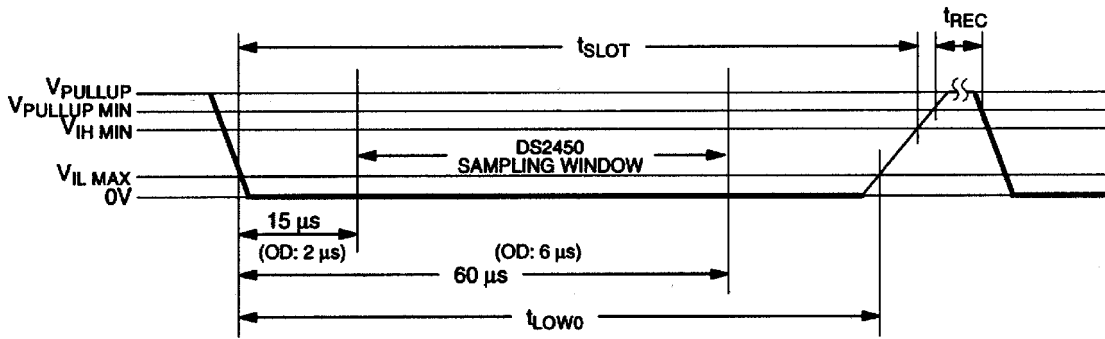
READ/WRITE TIME DIAGRAM Figure 11
Write-one Time Slot

	Regular Speed	Overdrive Speed
—— RESISTOR	$60\ \mu s \leq t_{SLOT} < 120\ \mu s$	$6\ \mu s \leq t_{SLOT} < 16\ \mu s$
—— MASTER	$1\ \mu s \leq t_{LOW1} < 15\ \mu s$	$1\ \mu s \leq t_{LOW1} < 2\ \mu s$
	$1\ \mu s \leq t_{REC} < \infty$	$1\ \mu s \leq t_{REC} < \infty$

READ/WRITE TIMING DIAGRAM Figure 11 (continued)
Write-zero Time Slot
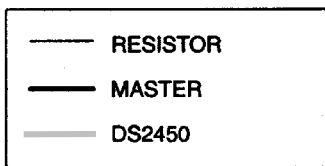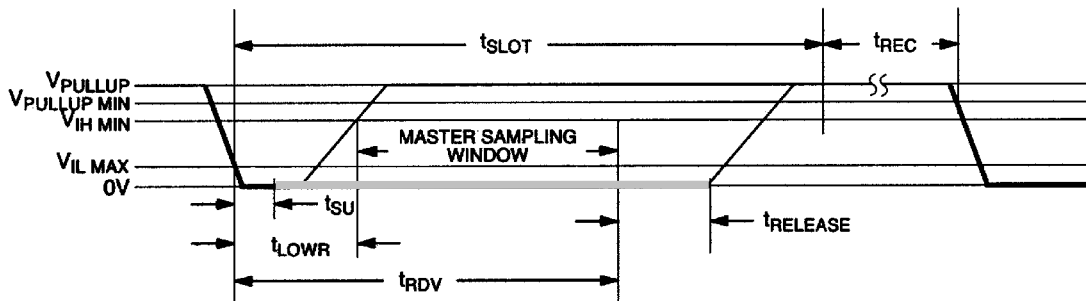

—— RESISTOR	
—— MASTER	

Regular Speed

$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Overdrive Speed

$6\ \mu s \le t_{LOW0} < t_{SLOT} < 16\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read-data Time Slot

—— RESISTOR	
—— MASTER	
—— DS2450	

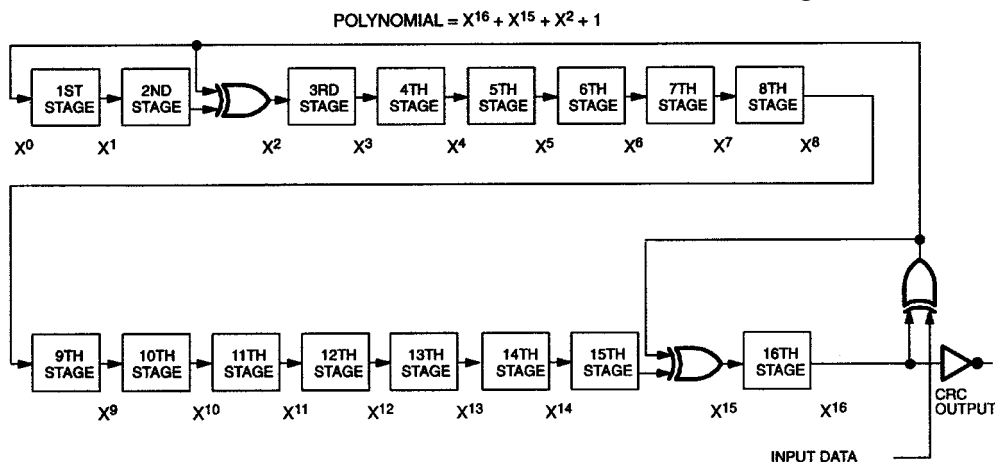**Regular Speed**

$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

$t_{SU} < 1\ \mu s$

Overdrive Speed

$6\ \mu s \le t_{SLOT} < 16\ \mu s$

$1\ \mu s \le t_{LOWR} < 2\ \mu s$

$0 \le t_{RELEASE} < 4\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 2\ \mu s$

$t_{SU} < 1\ \mu s$

CRC HARDWARE DESCRIPTION AND POLYNOMIAL Figure 12

POLYNOMIAL = $X^{16} + X^{15} + X^2 + 1$

CRC-GENERATION

With the DS2450 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is a 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2450 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non inverted) form when reading the ROM of the DS2450. It is computed once at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used to safeguard data when reading from or writing to the device's memory. It is the same type of CRC as is used with NV RAM based iButtons to safeguard data packets of the iButton File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned in the complemented (inverted) form. A CRC-generator inside the DS2450 chip (Figure 12) will calculate a new 16-bit CRC at every situation shown in the command flow chart of Figure 6.

The DS2450 provides this CRC value to the bus master to validate the transfer of command, address, and data to and from the bus master. When reading the memory, the 16-bit CRC is transmitted when the end of each 8-byte memory page is reached. At the initial pass through the Read Memory flow chart the 16-bit CRC will be generated by clearing the CRC-generator, shifting in the command byte, low address, high address and the data bytes beginning at the first addressed memory location and continuing until the last byte of the addressed memory page is reached. Subsequent passes through the Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC-generator and then shifting in the new data bytes starting at the first byte of the next page and continuing until the last byte of the page is reached.

When writing to the DS2450, the bus master receives a 16-bit CRC to verify the correctness of the data transfer before the device copies the data byte to its memory. With the initial pass through the Write Memory flow chart the 16-bit CRC will be generated by clearing the CRC-generator, shifting in the command, address low, address high and the data byte. Subsequent passes through the Write Memory flow chart due to the DS2450 automatically incrementing its address counter will generate an 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC-generator and then shifting in the new data byte.

For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx iButton Standards.

TRANSFER CHARACTERISTIC
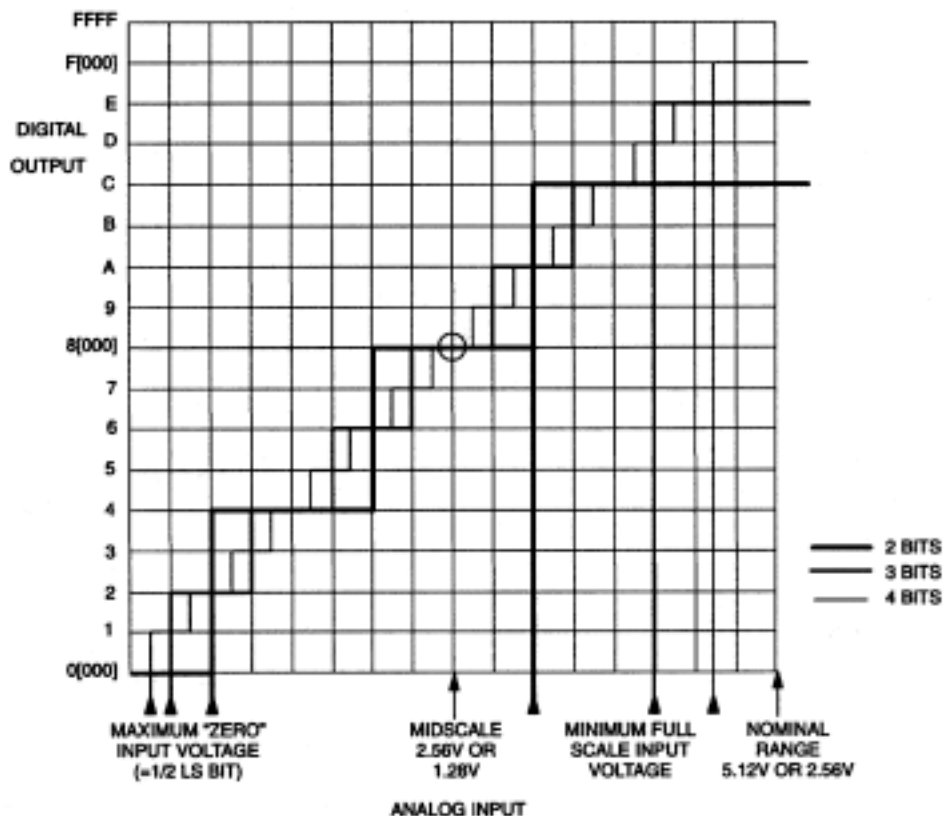
INCREMENT AND MINIMUM FULL SCALE INPUT VOLTAGE VERSUS RESOLUTION

	Range = 2.56V		Range = 5.12V	
Resolution	1 LS bit equivalent input voltage(mV)	minimum full scale input voltage (V)	1 LS bit equivalent input voltage (mV)	minimum full scale input voltage (V)
2 bits	640	1.60	1280	3.20
3 bits	320	2.08	640	4.16
4 bits	160	2.32	320	4.64
5 bits	80	2.44	160	4.88
6 bits	40	2.50	80	5.00
7 bits	20	2.53	40	5.06
8 bits	10	2.545	20	5.09
9 bits	5	2.5525	10	5.105
10 bits	2.5	2.5563	5	5.1125
11 bits	1.25	2.5581	2.5	5.1163
12 bits	0.625	2.5591	1.25	5.1181
13 bits	0.313	2.5595	0.625	5.1191
14 bits	0.156	2.5598	0.313	5.1195
15 bits	0.078	2.5599	0.156	5.1198
16 bits	0.039	2.5599	0.078	5.1199

In the shaded areas the accuracy is **less than** the resolution. The conversion results may include random noise.

ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} or V_{CC} =5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		μA	3
Operating Current	I_{CC}		0.5		mA	7
Quiescent Current	I_{CCQ}			20	μA	8

CAPACITANCE   (t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	5
Analog Input	C_{AIN}			50	pF	

RESISTANCES   (t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Analog Input	Z_{AIN}		1.0		MΩ	

AC ELECTRICAL CHARACTERISTICS REGULAR SPEED
(V_{PUP}=4.0V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW}	1		15	μs	
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Low Time	t_{LOWR}	1		15	μs	
Read Data Valid	t_{RDV}		exactly 15		μs	
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	4
Recovery Time	t_{REC}	1			μs	
Reset Time High	t_{RSTH}	480			μs	
Reset Time Low	t_{RSTL}	480			μs	6
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	

AC ELECTRICAL CHARACTERISTICS
OVERDRIVE SPEED $(V_{PUP} = 4.0V$ to $6.0V$; $-40°C$ to $+85°C)$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	
Read Data Valid	t_{RDV}		Exactly 2		µs	
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	4
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDH}	2		6	µs	
Presence Detect Low	t_{PDL}	8		24	µs	

AC ELECTRICAL CHARACTERISTICS $(V_{PUP}$ or $V_{CC} = 5V \pm 10\%$; $-40°C$ to $+85°C)$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Sample & Hold Aperture	t_{SH}		20		µs	
Equivalent Input Noise	V_{INOISE}		t.b.d.		µV RMS	
Total Conversion Error	N_{ERR}		$\pm 1/2$		LSB	9

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pullup voltage.

3. Input load is to ground.

4. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

5. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{PUP}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

6. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

7. Measured with $V_{CC} = 5.0V$ supply and 1-Wire input open.

8. Measured with $V_{CC} = 5.0V$ supply, 1-Wire input open and analog circuitry inactive.

9. At 8-bit resolution regardless of range and temperature; includes offset, non-linearity and noise.